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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,394	04/15/2004	Kotaro Kataoka	1248-0713PUS1	6400

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,394	KATAOKA ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/10/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-26** are currently pending in the application.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in JAPAN, 2003-141877 on 05/20/2003.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 08/10/2004. The references cited on the PTOL 1449 form have been considered.

Specification

The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

Claims **1-2, 14 and 15** are objected to because of the following reasons.

In claim **1**, lines 5-8 "a gate insulating film ... provided on a p-type semiconductor substrate, a p-type well region in a semiconductor substrate, or an insulator" should read – a gate

insulating film ... provided on the p-type semiconductor substrate, the p-type well region in the semiconductor substrate, or the insulator--.

In claim **2**, "wherein the p-type semiconductor film provided on a p-type semiconductor substrate, a p-type well region in a semiconductor substrate, or an insulator ..." should read – wherein the p-type semiconductor film provided on the p-type semiconductor substrate, the p-type well region in the semiconductor substrate, or the insulator ...--.

In claim **14**, lines 5-8 "a gate insulating film ... provided on a n-type semiconductor substrate, a n-type well region in a semiconductor substrate, or an insulator" should read – a gate insulating film ... provided on the p-type semiconductor substrate, the n-type well region in the semiconductor substrate, or the insulator--.

In claim **15**, "wherein the n-type semiconductor film provided on a n-type semiconductor substrate, a n-type well region in a semiconductor substrate, or an insulator ..." should read – wherein the n-type semiconductor film provided on the n-type semiconductor substrate, the n-type well region in the semiconductor substrate, or the insulator ...--.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1, 3-7, 9-12** are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa (USP 6,335,554).

Regarding Claim 1, Yoshikawa discloses in Figs. 1-2C and corresponding texts as set forth in column 6, line 20-column 7, line 30, a semiconductor memory, comprises:

a p-type semiconductor film provided on a p-type semiconductor substrate 1, a p-type well region in a semiconductor substrate, or an insulator;

a gate insulating film 2 formed on the p-type semiconductor film provided on the p-type semiconductor substrate, the p-type well region in the semiconductor substrate , or the insulator;

a gate electrode 3 formed on the gate insulating film;

two charge storage sections 4a, 4b formed on side walls of the gate electrode;

a channel region provided below the gate electrode; and

a first n-type diffusion layer region 11 and a second n-type diffusion layer region 11 provided to sides of the channel region,

wherein :

the charge storage sections are arranged to change an electric current flow between the first n-type diffusion layer region and the second n-type diffusion layer region under application of a voltage to the gate electrode according to a quantity of electric charge stored the charge storage sections; and

the first n-type diffusion layer region is set to a reference voltage S, Ground (Fig. 2A), the second n-type diffusion layer region is set to voltage D, 8V (Fig. 2A) greater than the reference voltage, and the gate electrode is set to a voltage G, 10V (Fig. 2A) greater than the reference voltage, so as inject electrons to one of the charge storage sections near the second n-type diffusion layer region.

Regarding Claim **3**, Yoshikawa discloses in Figs. 1-2C the first and second n-type diffusion layer regions have an offset structure where the gate electrode does not overlap the first and second n-type diffusion layer regions with the gate insulating film intervening therebetween.

Regarding Claim **4**, Yoshikawa discloses in Figs. 1-2C the charge storage sections overlap the channel region between the first n-type diffusion layer region and the second n-type diffusion layer region.

Regarding Claims **5 and 6**, Yoshikawa discloses in Figs. 1-2C the charge storage sections include a charge storing film 6 capable of storing charge, a first insulating film 5, and a second insulating film 7; and the charge storage sections have a structure where the charge storing film is sandwiched between the first insulating film and the second insulating film; wherein the charge storing film is made of silicon nitride; and the first and second insulating films are made of a silicon oxide.

Regarding Claim 7, Yoshikawa discloses in Figs. 1-2C the first insulating film 5 separates the charge storing film from the channel region or a well region; and above the channel region, the first insulating film is 10 nm thick and is thinner than the gate insulating film 2 of 25 nm (col. 7, line 35 and col. 7, line 50).

Regarding Claims **9-11**, Yoshikawa discloses in Figs. 1-2C the charge storing film has a part having a surface substantially parallel to a surface of the gate insulating film; the charge storing film has a part extending substantially parallel to a side face of the gate electrode; the charge storing film has a part having a surface substantially parallel to a surface of the gate insulating film and also has a part extending substantially parallel to a side face of the gate electrode.

Regarding Claim **12**, Yoshikawa discloses in Figs. 1-2C the charge storage sections at least partly overlap part of the n-type diffusion layer regions.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim **2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa (USP 6,335,554) in view of Atsumi et al. (USP 5,438,542 hereinafter referred to as "Atsumi").

Yoshikawa discloses all the claimed limitations except for the p-type semiconductor film provided on a p-type semiconductor substrate, a p-type well region in a semiconductor substrate, or an insulator is set to a voltage less than the reference voltage. Atsumi teaches that a semiconductor memory device allows collective data writing by means of substrate hot electrons by controlling the biased condition of the related voltage as shown in Fig. 16. If the control gate voltage Vg of the memory cell is 10V, the substrate voltage Vsub is −10V and the source/reference voltage Vs is 0V, the voltage to be applied to the transistors constituting a peripheral circuit is held as low as 10V for collective data writing by means of substrate hot electrons, that can improve the efficiency η of injecting electrons into the floating gate (η=gate current/substrate current) as compared with injection of channel hot electrons. This technique allows simultaneous data writing for a plurality of memory cells to reduce the time required for a erasing/writing cycle test and for data writing before data erasure as set forth in column 8, lines

25-46. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of collective data writing by means of substrate hot electrons technique by controlling the biased condition of the related voltage as shown in Fig. 16, as taught by Atsumi to incorporate into Yoshikawa's the semiconductor memory to set a voltage of the substrate (-10V) less than the reference/source voltage (0V) in order to improve the efficiency of injecting electrons and allow simultaneous data writing for a plurality of memory cells to reduce the time required for a erasing/writing cycle test and for data writing before data erasure.

Claims **8, 14-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa (USP 6,335,554).

Regarding Claims **8 and 21**, Yoshikawa discloses in Figs. 1-2C the first insulating film 5 separates the charge storing film from the channel region or a well region; and above the channel region, the first insulating film is 10 nm thick and the gate insulating film 2 of 25 nm except for the first insulating film is at most 20 nm thick and is thicker than the gate insulating film. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the first insulating film is at most 20 nm thick and is thicker than the gate insulating film, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claims **14-17 and 25**, Yoshikawa discloses all the claimed limitations as above except for reversed impurities. It would have been obvious to one of ordinary skill in the

art at the time of the invention was made to reverse impurities to arrive the claimed limitations since it was known in the art reversing impurity that involves only routine skill in the art.

Regarding Claims **18 and 19**, Yoshikawa discloses in Figs. 1-2C the charge storage sections include a charge storing film 6 capable of storing charge, a first insulating film 5, and a second insulating film 7; and the charge storage sections have a structure where the charge storing film is sandwiched between the first insulating film and the second insulating film; wherein the charge storing film is made of silicon nitride; and the first and second insulating films are made of a silicon oxide.

Regarding Claim **20**, Yoshikawa discloses in Figs. 1-2C the first insulating film 5 separates the charge storing film from the channel region or a well region; and above the channel region, the first insulating film is 10 nm thick and is thinner than the gate insulating film 2 of 25 nm (col. 7, line 35 and col. 7, line 50).

Regarding Claims **22-24**, Yoshikawa discloses in Figs. 1-2C the charge storing film has a part having a surface substantially parallel to a surface of the gate insulating film; the charge storing film has a part extending substantially parallel to a side face of the gate electrode; the charge storing film has a part having a surface substantially parallel to a surface of the gate insulating film and also has a part extending substantially parallel to a side face of the gate electrode.

Claims **13 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa (USP 6,335,554) in view of Eitan (USP 6,348,711).

Yoshikawa discloses all the claimed limitations except for the semiconductor memory further comprises n-type high concentration regions, adjacent to channel region sides of the p-type diffusion layer regions, which have a greater p-type impurity concentration than the channel region. Eitan teaches in Fig. 4A that an NROM cell comprises p-type high concentration regions/a Boron implant 120, adjacent to channel region 100 sides of the n-type diffusion layer regions 102, 104, which have a greater p-type impurity concentration than the channel region. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teaching of forming p-type high concentration regions/a Boron implant, adjacent to channel region sides of the n-type diffusion layer regions, which have a greater p-type impurity concentration than the channel region, as taught by Eitan to incorporate into Yoshikawa's the semiconductor memory to include p-type high concentration regions/a Boron implant, adjacent to channel region sides of the n-type diffusion layer regions, which have a greater p-type impurity concentration than the channel region in order to have a maximum concentration near the diffusion layer region (col. 5, lines 40-41). For a PROM cell, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to reverse impurities of NROM to form PROM since it was known in the art reversing impurity that involves only routine skill in the art.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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06/23/05

Andy Huynh

Patent Examiner